CERTIFICATE OF MAILING UNDER 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 16, 2006.

Sue Bromaghim May 16, 2006

CUSTOMER NO. 36257

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Gerrit Jan HEMINK		
Title:	Self-Boosting System for Flash Memory Cells		
Application No.:	10//774,014	Filing Date:	February 6, 2004
Examiner:	Michael Thanh TRAN	Group Art Unit:	2827
Docket No.:	SNDK.327US0	Conf. No.:	8419

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

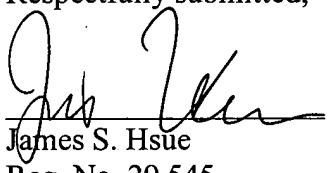
Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant(s) call(s) the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application.

☒ According to 37 C.F.R. 1.98(2)(ii), copies of the U.S. Patents and U.S. Published Patent Applications documents are not required and are therefore not enclosed. Copies of the listed foreign patent documents or Other Art are enclosed.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(b) and consequently no fee should be required. The Commissioner is authorized, however, to charge any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664.

Respectfully submitted,



May 16, 2006
Date

James S. Hsue
Reg. No. 29,545

PARSONS HSUE & DE RUNTZ LLP
595 Market Street, Suite 1900
San Francisco, CA 94105
(415) 318-1160 (main)
(415) 318-1162 (direct)
(415) 693-0194 (fax)

U.S. Department of Commerce, Patent and Trademark	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	SNDK.327US0	10/774,014
	Applicants	**Conf. No.**
(Use several sheets if necessary)	Gerrit Jan HEMINK	8419
(Form PTO-1449)	**Filing Date**	**Art Group**
	February 6, 2004	2827

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	1	5,677,873	10-1997	Choi et al.			
	2	5,793,677	08-1998	Hu et al.			
	3	5,969,985	10-1999	Tanaka et al.			
	4	5,991,202	11-1999	Derhacobian et al.			
	5	6,044,013	03-2000	Tanaka et al.			
	6	6,061,270	05-2000	Choi			
	7	6,154,391	11-2000	Takeuchi et al.			
	8	6,282,117 B1	08-2001	Tanaka et al.			
	9	6,363,010 B2	03-2002	Tanaka et al.			
	10	6,493,265 B2	12-2002	Satoh et al.			
	11	6,545,909 B2	04-2003	Tanaka et al.			
	12	6,717,861 B2	04-2004	Jeong et al.			
	13	6,859,394 B2	02-2005	Matsunaga et al.			
	14	6,859,395 B2	02-2005	Matsunaga et al.			
	15	6,930,921 B2	08-2005	Matsunaga et al.			

U.S. Published Patent Application Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	16	2005/0047210 A1	03-2005	Matsunaga et al.			
	17	2005/0174852 A1	08-2005	Hemink			
	18	2005/0226055 A1	10-2005	Guterman			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark	**Atty. Docket No.**	**Application No.**
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	SNDK.327US0	10/774,014
	Applicants	**Conf. No.**
(Use several sheets if necessary)	Gerrit Jan HEMINK	8419
(Form PTO-1449)	**Filing Date**	**Art Group**
	February 6, 2004	2827

U.S. Patent Documents								

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
	19	Choi et al., "A Novel Booster Plate Technology in High Density NAND Flash Memories for Voltage Scaling Down and Zero Program Disturbance", 1996 Symposium on VLSI Technology Digest of Technical Papers, 0-7803-3342-X/96/IEEE, 4 pages.
	20	Kim et al., "Fast Parallel Programming of Multi-Level NAND Flash Memory Cells Using the Booster-Line Technology", Symposium on VLSI Technology Digest of Technical Papers, (1997), 2 pages.
	21	Brown et al., Editors, "Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide to Understanding and Using NVSM Devices", IEEE Press Series on Microelectronic Systems, (1998), 57 pages.
	22	Cho et al., "A Dual Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single-Level Modes", IEEE Journal of Solid-State Circuits, Vol. 36, No. 11, Nov. 2001, 9 pages.
	23	Satoh et al., "A Novel Gate-Offset NAND Cell (GOC-NAND) Technology Suitable for High-Density and Low-Voltage Operation Flash Memories", IEDM Technical Digest, Dec. 1999, 6 pages.
	24	Jung et al., "A 3.3-V Single Power Supply 16-Mb Nonvolatile Virtual DRAM Using a NAND Flash Memory Technology", IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, Nov. 1997, 12 pages.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.